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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,665	05/21/2004	Hsin-Wo Fang	NAUP0592USA	3664

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EXAMINER	
ROSSOSHEK, YELENA	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 07/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,665	FANG ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-12,14 and 15* is/are rejected.

7)☒ Claim(s) *6 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/709,665 filed 05/21/2004.

2. Claims 1-15 are pending in the Application.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-5, 7-12, 14 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Schadt et al. (US Patent 6,870,395).

With respect to claim 1 Schadt et al. teaches a method for implementing circuit layouts in a chip (within a layout of the chip/PLD shown on the Fig. 2 (col. 3, ll.31-32)), comprising: forming a plurality of sub-circuit cells with the same layout in different positions of the chip (within plurality of standard-cell logic blocks (SLBs) 220 as shown on the Fig. 2 (col. 3, ll.40-42), wherein SLBs are construed by same type of standard-cell logic, i.e. having the same layout (col. 4, ll.3-5) and are placed in different positions of the PLD (col. 4, ll.9-10)); and when the sub-circuit cells in different positions require different circuit functions, performing a layout programming in at least a connection layer so that different layouts are formed in different positions of the connection layer

corresponding to the sub-circuit cells (within placing SLBs in different areas of PLD depending on the functionality to be supported (col. 4, ll.6-8) and using two types of connectivity structure in order to integrated SLBs with the rest of the chip (col. 4, ll.42-44), wherein both types of connectivity structure are using upper layer of metallization (metal layer) programmably connect each SLB to the other portions of the chip/PLD as shown on the Fig. 9 (col. 4, ll.44-56)).

With respect to claim 9 Schadt et al. teaches a chip (within a layout of the chip/PLD shown on the Fig. 2 (col. 3, ll.31-32)), comprising: a plurality of layout layers comprising a plurality of same layouts in a plurality of positions of the layout layers so as to implement a plurality of sub-circuit cells with the same layout (within multilayered PLD (col. 4, ll.53-54) containing plurality of SLBs 220 as shown on the Fig. 2 having the same layout of standard-cell blocks in different positions of the PLD 200 around the periphery of the device (i.e. within I/O ring) (col. 3, ll.40-42), wherein SLBs can placed anywhere within PLD/chip (col. 4, ll.9-10); and at least a connection layer comprising different layouts corresponding to the different positions of the layout layers so that the sub-circuit cells in different positions implement different circuit functions (within programmable connection of each SLB with the other portions of the PLD (col. 4, ll.51-53) using metal layers of the PLD (col. 4, ll.53-55) depending on the available area and the functionality to be supported (col. 4, ll.6-8)).

With respect to claims 2-5, 7, 8, 10-12, 14 and 15 Schadt et al. teaches:

Claims 2, 10: wherein the connection layer is a metal layer (col. 4, ll.53-55);

Claim 3: the layout programming is only performed in the connection layer so that the sub-circuit cells with different circuit functions have different layouts only in the connection layer (within SLBs construed by the same type of standard-cell logic blocks (col. 4, ll.4-6), wherein in order to support different functions SLBs have programmable connectivity structure (col. 4, ll.44-52) without changing the layout of SLBs));

Claims 4, 11: wherein while forming the plurality of sub-circuit cells with the same layout, a plurality of sub-circuit blocks are laid in each sub-circuit cell, wherein while performing the layout programming, each layout in the connection layer corresponding to each sub-circuit cell is selectively connected to the sub-circuit blocks of each sub-circuit cell so that the sub-circuit cells in different positions implement different circuit functions (within plurality of SLBs construed by the same type of multiple standard-cell logic (col. 4, ll.4-6), wherein SLBs can perform different functions depending on programmable connectivity structure using routing resources (col. 4, ll.61-65) using switch boxes, which can be programmed to provide signal flow in a variety of ways between SLB 220 and the rest of the PLD (col. 5, ll.8-13));

Claims 5, 12: wherein the sub-circuit cells in different positions are for implementing input/output (I/O) circuits with different I/O functions (using plurality of SLBs positioned around the periphery of the device layout, i.e. in the I/O ring (col. 1, ll.51-53) for performing programmable connections between I/O circuitry and the programmable core logic of the chip (col. 2, ll.1-3);

Claims 7, 14: wherein the sub-circuit cells in different positions are for implementing I/O circuits with different slew rates (within different type of SLBs performing different functions (col. 9, ll.26-27; ll.43-47; col. 10, ll.58-67));

Claims 8, 15: wherein the sub-circuit cells in different positions are for implementing I/O circuits with different driving currents (within different type of SLBs performing different functions (col. 9, ll.26-27; ll.43-47; col. 10, ll.58-67)).

Allowable Subject Matter

5. Claims 6 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach implementation I/O circuits with a Schmidt trigger function with the sub-circuit cells in different positions as claimed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Examiner
Helen Rossoshek
AU 2825

SUN JAMES LIN
PRIMARY EXAMINER